takeMS

the Speed you Need

Technical Datasheet

BD256TEC400 (256MB / PC3200)

BD512TEC500 (512MB / PC3200)

Rev. 1.1 / Breisach, 07/2005

DESCRIPTION

The takeMS 184pin DDR SDRAM DIMM series is unbuffered 184-pin double data rate Synchronous DRAM Dual In-Line Memory Modules which are organized as 32/64Mx64 high-speed memory arrays. The modules (Single Side or Double Side) consists of eight or sixteen 32Mx8 DDR SDRAM in 400mil TSOP II packages on a 184pin glass-epoxy substrate. It is suitable for easy interchange and addition.

The takeMS 184pin DDR SDRAM DIMM series is designed for high speed of up to 200MHz and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data(DQ), Data strobes(DQS) and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

The takeMS 184pin DDR SDRAM DIMM series incorporates SPD (serial presence detect).

Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by takeMS to identify DIMM type, capacity and other information of DIMM.

FEATURES

* 256/512MB Unbuffered DDR DIMM based on 32Mx8 DDR SDRAM
* JEDEC Standard 184pin dual in-line memory module(DIMM)
* Data inputs on DQS centers when write (centered DQ)
* Data strobes synchronized with output data for read & input data for write
* All inputs & outputs are compatible with SSTL_2 interface
* Fully differential clock operations (CLK & CLK) with 200MHz
* All addresses & control inputs except Data, Data strobes & Data masks latched on the rising edges of the clock
* Data(DQ), Data strobes & Write masks latched on both rising & falling edges of the clock
* 2.6V +/- 0.2V VDD & VDDQ Power supply
* Programmable CAS Latency 2 /2.5 supported
* Internal four bank operations with single pulsed RAS
* Auto refresh& self refresh supported
* Programmable Burst Length 2/4/8 with both sequential 7 interleave mode
* 4096 refresh cycles / 64ms

Clock Frequency	Interface	Power Supply	SDRAM Package
200MHz (PC3200) DDR 400 CL2.5=200 DDR 333 CL2.5=166 DDR 266 CL2=133	SSTL_2	VDD=2.6V VDDQ=2.6V	400mil 66pin TSOP II

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32/64Mx64 bits
184PIN PC3200 DDR SDRAM DIMM

184 PIN 64 BIT DDR SDRAM DIMM

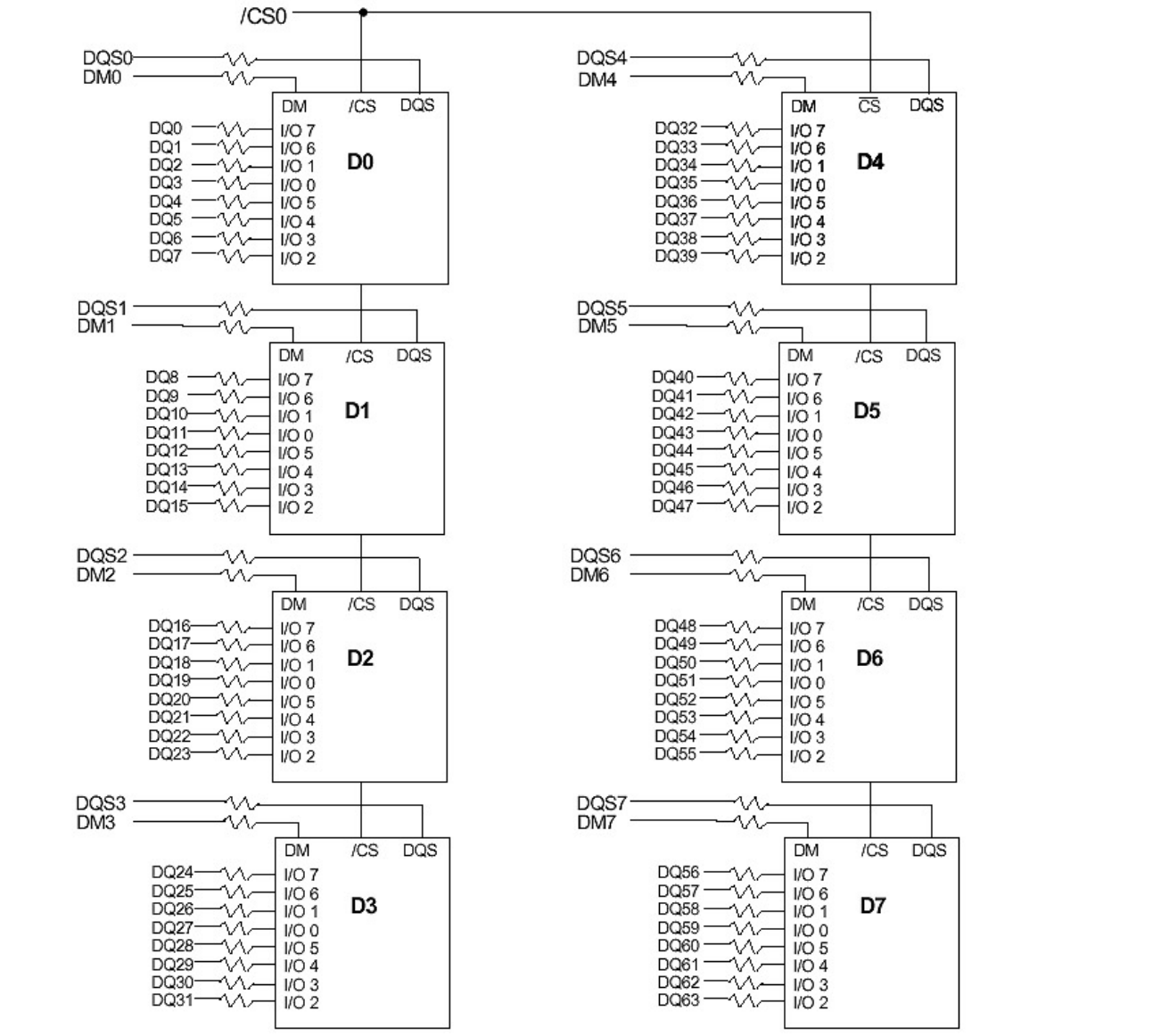
PIN DESCRIPTION

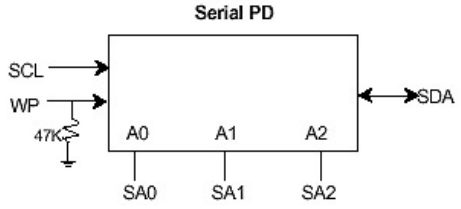
Pin	Pin Description	Pin	Pin Description
CK0,/CK0,CK1,/CK1,CK2,/CK2	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0	Chip Select Input	VSS	Ground
CKE0	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAAS, /WE	Command Sets Inputs	VDDSPD	Power Supply for SPD
A0 – A11	Address	SA0 – SA2	EEPROM Address Inputs
BA0, BA1	Bank Address	SCL	EEPROM Clock
DQ0 – DQ63	Data Inputs/Outputs	SDA	EEPROM Data I/O
DQS0 – DQS7	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0 – DM7	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

PIN ASSIGNMENT

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	A13*	134	CB4*	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5*	165	DQ52
13	DQ9	44	CB0*	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1*	75	/CK2	106	DQ13	137	CK1	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK1	168	VDD
16	CKO	47	DQS8*	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK0	48	A0	78	DQS6	109	DQ14	140	DM8*	170	DQ54
18	VSS	49	CB2*	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6*	172	VDDQ
20	DQ11	51	CB3*	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7*	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12*	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQA8	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

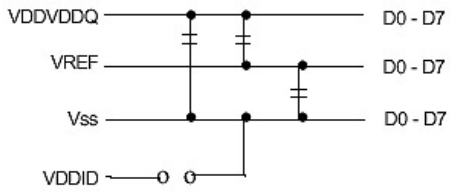
BLOCK DIAGRAM





Clock Wiring	
Clock Input	SDRAMs
*CK0,/CK0	2 SDRAMs
*CK1,/CK1	3 SDRAMs
*CK2,/CK2	3 SDRAMs

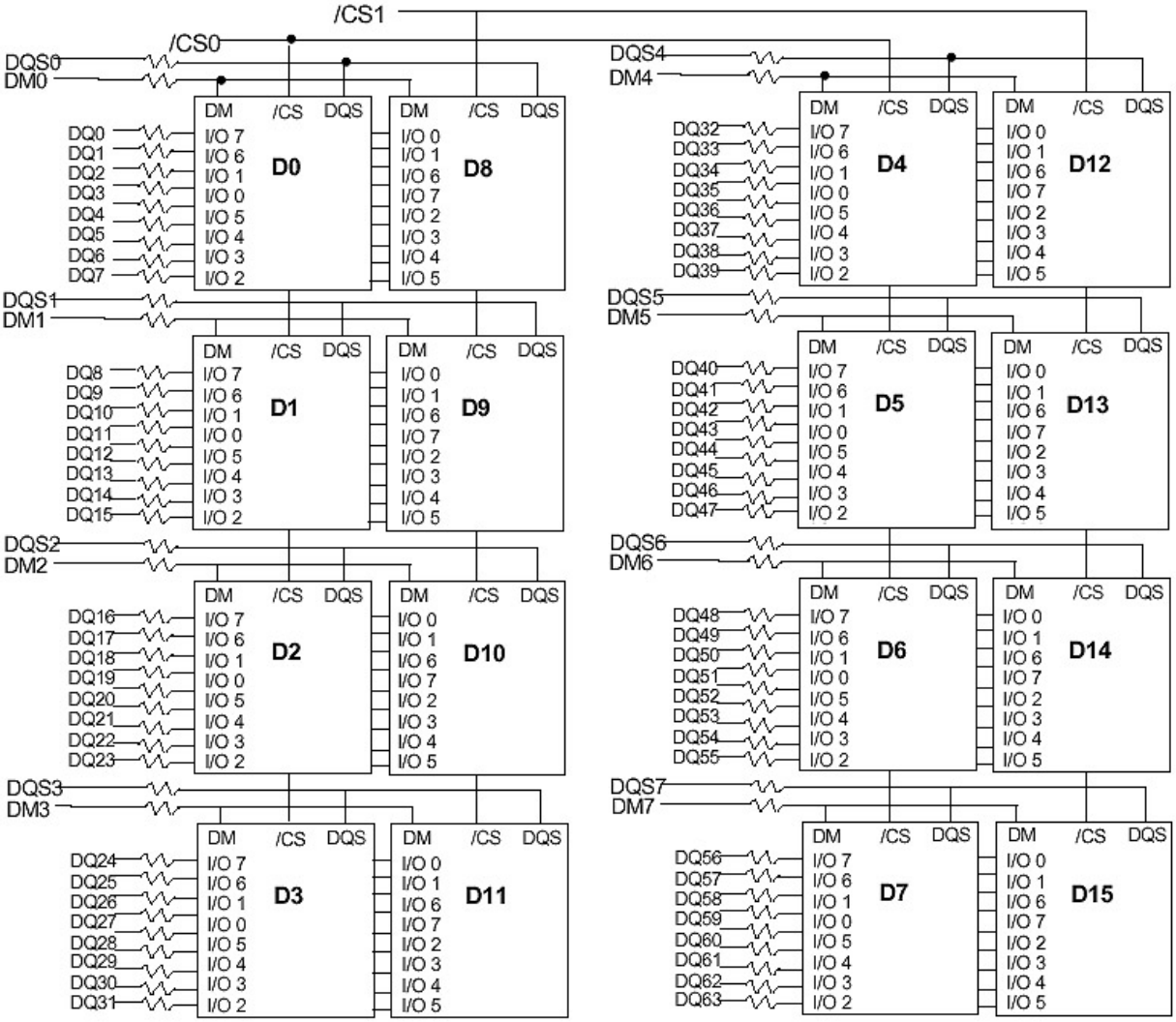
* Wire per clock loading table/wiring diagrams

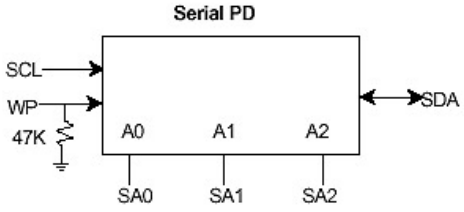


BA0-BA1 → BA0-BA1 : SDRAMs D0 - D7
A0 - A11 → A0 - A11 : SDRAMs D0 - D7
/RAS → /RAS : SDRAMs D0 - D7
/CAS → /CAS : SDRAMs D0 - D7
CKE0 → CKE : SDRAMs D0 - D7
/WE → /WE : SDRAMs D0 - D7

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ,DQS, DM/DQS resistors : 22 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ) :
   Strap out :(open) : VDD=VDDQ
   Strap In (Vss) : VDD≠VDDQ

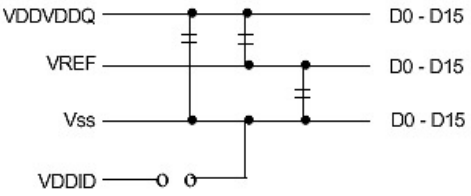
BLOCK DIAGRAM





Clock Wiring	
Clock Input	SDRAMs
*CK0,/CK0	4 SDRAMs
*CK1,/CK1	6 SDRAMs
*CK2,/CK2	6 SDRAMs

* Wire per clock loading table/wiring diagrams



BA0-BA1 → BA0-BA1 : SDRAMs D0 - D15
A0 - A11 → A0 - A11 : SDRAMs D0 - D15
CKE1 → CKE1 : SDRAMs D8 - D15
/RAS → /RAS : SDRAMs D0 - D15
/CAS → /CAS : SDRAMs D0 - D15
CKE0 → CKE : SDRAMs D0 - D7
/WE → /WE : SDRAMs D0 - D15

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ,DQS, DM/DQS resistors : 22 Ohms.
4. VDDID strap connections
   (for memory device VDD, VDDQ) :
   Strap out :(open) : VDD=VDDQ
   Strap In (Vss) : VDD≠VDDQ

184 PIN x64 DDR SDRAM DIMM, 2 Bank with x8 DDR SDRAMs

Electrical Characteristics

Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	–	V_{DDQ} + 0.5	V	–
Voltage on Inputs relative to V_{SS}	V_{IN}	-0.5	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5	–	+3.6	V	–
Operating Temperature (Ambient)	T_A	0	–	+70	°C	–
Storage Temperature	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short Circuit Output Current	I_{OUT}	–	50	–	mA	–

Attention: Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to recommended operation conditions. Exceeding only one of these values for extended periods of time affect device reliability and may cause irreversible damage to the integrated circuit.

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Note/ Test Condition
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	f_{CK} ≤166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz 1)
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	f_{CK} ≤166 MHz 2)
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz 1)2)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	f_{CK} ≤166 MHz 3)
Input Reference Voltage	V_{REF}	V_{DDQ} / 2 –50 mV	V_{DDQ} / 2	V_{DDQ} / 2 + 50 mV	V	f_{CK} > 166 MHz 1)3)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	4)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—

1) DDR400 conditions apply for all clock frequencies above 166 MHz

2) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

3) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

4) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

Parameter	Symbol	Values		Unit	Note/ Test Condition [1]
		min.	max.		
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.15	V_{DDQ} + 0.3	V	[2]
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	V_{REF} – 0.15	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	[3]
Output Leakage Current	I_{OL}	– 5	5	µA	[3]

1) V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS}

2) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\,(max.)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

3) For any pin under test input of 0 V ≤VIN ≤V_{DDQ} + 0.3 V. Values are shown per DDR SDRAM component

AC Timing - Absolute Specifications

Parameter	Symbol	DDR400		Unit	Note/ Test Condition [1]
		Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.6	+0.6	ns	[2)3)4)5)]
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.5	+0.5	ns	[2)3)4)5)]
CK high-level width	t_{CH}	0.45	0.55	t_{CK}	[2)3)4)5)]
CK low-level width	t_{CL}	0.45	0.55	t_{CK}	[2)3)4)5)]
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		ns	[2)3)4)5)]
Clock cycle time	t_{CK}	5	12	ns	CL = 3.0 [2)3)4)5)]
		6	12	ns	CL = 2.5 [2)3)4)5)]
		7.5	12	ns	CL = 2.0 [2)3)4)5)]
DQ and DM input hold time	t_{DH}	0.4	—	ns	[2)3)4)5)]
DQ and DM input setup time	t_{DS}	0.4	—	ns	[2)3)4)5)]
Control and Addr. input pulse width (each input)	t_{IPW}	tbd	—	ns	[2)3)4)5)6)]
DQ and DM input pulse width (each input)	t_{DIPW}	tbd	—	ns	[2)3)4)5)6)]
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.6	+0.6	ns	[2)3)4)5)7)]
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.6	+0.6	ns	[2)3)4)5)7)]
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	t_{CK}	[2)3)4)5)]
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	ns	TSOPII [2)3)4)5)]
Data hold skew factor	t_{QHS}	—	+0.50	ns	TSOPII [2)3)4)5)]
DQ/DQS output hold time	t_{QH}	t_{HP} – t_{QHS}	—	ns	[2)3)4)5)]
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	[2)3)4)5)]

AC Timing - Absolute Specifications (cont'd)

Parameter	Symbol	DDR400		Unit	Note/ Test Condition [1]
		Min.	Max.		
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.6	—	ns	fast slew rate 3)4)5)6)10)
		NA		ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.6	—	ns	fast slew rate 3)4)5)6)10)
		NA		ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	65	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	15	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	10	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}			t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.6 V ±0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

Serial Presence Detect

256M Bytes for Unbuffered & Non ECC Module (DDR400 use 32Mx8 *8pcs)			
Byte No.	**Description**	**Function**	**Hex Value**
0	Number of Serial PD Bytes used	128 bytes	80h
1	Total number of Bytes in Serial PD device	256 bytes	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	# of Row Addresses on this assembly	13	0Dh
4	# of Column Addresses on this assembly	10	0Ah
5	# of Physical Banks on DIMM	1 ROWS	01h
6	Data Width of this assembly	64 bit	40h
7	Data Width of this assembly(Continued)	0	00h
8	Voltage Interface Level of this assembly	SSTL_2.5V	04h
9	DDRAM Cycle time at CAS Latency=2.5	5 ns	50h
10	DDRAM Access from Clock at CAS Latency=2.5	+/- 0.7 ns	70h
11	DIMM configuration type(Non-parity, Parity or ECC)	Non-parity	00h
12	Refresh Rate/Type	7.8 us	82h
13	Primary SDRAM Width	X8 bit	08h
14	Error Checking SDRAM Width	None	00h
15	Min. Clock Delay, Back-to-Back Random Column Access	Tccd=1 clk	01h
16	Burst Lengths Supported	2,4,8	0eh
17	Number of Banks on SDRAM Device	4 Banks	04h
18	CAS Latency	2.5	08h
19	Chip Select Latency	0 clk	01h
20	Write Latency	1 clk	02h
21	DDR SDRAM Module Attributes	Unbuffer	20h
22	DDRAM Device Attributes: General	+/- 0.2v voltage tolerance	00h
23	DDRAM Cycle time at CAS Latency=2	7.5ns	75h
24	DDRAM Access from Clock at CAS Latency=2	+/- 0.7 ns	70h
25	DDRAM Cycle time at CAS Latency=1.5	None	00h
26	DDRAM Access from Clock at CAS Latency=1.5	None	00h
27	Minimum Row Precharge Time (tRP)	15 ns	3Ch
28	Minimum Row Active to Row Active delay (tRRD)	10 ns	28h
29	Minimum RAS to CAS delay (tRCD)	15 ns	3Ch
30	Minimum Active to Precharge Time (tRAS)	40 ns	28h
31	Module Bank Density	256M of 1 row	40h
32	Address and Command Input Setup Time Before Clock	0.6 ns	60h
33	Address and Command Input Hold Time After Clock	0.6 ns	60h
34	Data/Data Mask Input Setup Time Before Data Strobe	0.4 ns	40h
35	Data/Data Mask Input Hold Time After Data Strobe	0.4 ns	40h
36-40	Reserved	Reserved	00h
41	Minimum active /auto-refresh time(tRC)	55 ns	37h
42	Minimum auto-refresh to active command period (tRFC)	70 ns	46h
43	Maximum cycle time(Tck max)	10 ns	28h
44	Maximum DQS-DQ skew time(tDQSQ)	0.4 ns	28h
45	Maximum read data hold skew factor(tQHS)	0.50 ns	50h
46-61	Reserved	Reserved	00h
62	SPD Revision	Rev0.0	00h
63	Checksum for Bytes 0-62	-	BDh
64-71	Manufacturer’s JEDEC ID Code	-	7F, 7F, 7F, 58h
72	Module Manufacturing Location	-	31h
73-90	Module Part Number	BD256TEC400	42, 44, 32, 35, 36, 54, 45, 43, 34, 30, 30h
91-92	Module Revision Code	Reserved	00h
93-94	Module Manufacturing Date	YY-WW	-
95-98	Module Serial Number	Reserved	00h
99-127	Manufacturer’s Specific Data	Reserved	00h
128-255	Open for customer use	Reserved	00h

Serial Presence Detect

512M Bytes for Unbuffered & Non ECC Module (DDR400 use 32Mx8 *16pcs)			
Byte No.	**Description**	**Function**	**Hex Value**
0	Number of Serial PD Bytes used	128 bytes	80h
1	Total number of Bytes in Serial PD device	256 bytes	08h
2	Fundamental Memory Type	DDR SDRAM	07h
3	# of Row Addresses on this assembly	13	0Dh
4	# of Column Addresses on this assembly	10	0Ah
5	# of Physical Banks on DIMM	2 ROWS	02h
6	Data Width of this assembly	64 bit	40h
7	Data Width of this assembly(Continued)	0	00h
8	Voltage Interface Level of this assembly	SSTL_2.5V	04h
9	DDRAM Cycle time at CAS Latency=2.5	5 ns	50h
10	DDRAM Access from Clock at CAS Latency=2.5	+/- 0.7 ns	70h
11	DIMM configuration type(Non-parity, Parity or ECC)	Non-parity	00h
12	Refresh Rate/Type	7.8 us	82h
13	Primary SDRAM Width	X8 bit	08h
14	Error Checking SDRAM Width	None	00h
15	Min. Clock Delay, Back-to-Back Random Column Access	Tccd=1 clk	01h
16	Burst Lengths Supported	2,4,8	0eh
17	Number of Banks on SDRAM Device	4 Banks	04h
18	CAS Latency	2.5	08h
19	Chip Select Latency	0 clk	01h
20	Write Latency	1 clk	02h
21	DDR SDRAM Module Attributes	Unbuffer	20h
22	DDRAM Device Attributes: General	+/- 0.2v voltage tolerance	00h
23	DDRAM Cycle time at CAS Latency=2	7.5ns	75h
24	DDRAM Access from Clock at CAS Latency=2	+/- 0.7 ns	70h
25	DDRAM Cycle time at CAS Latency=1.5	None	00h
26	DDRAM Access from Clock at CAS Latency=1.5	None	00h
27	Minimum Row Precharge Time (tRP)	15 ns	3Ch
28	Minimum Row Active to Row Active delay (tRRD)	10 ns	28h
29	Minimum RAS to CAS delay (tRCD)	15 ns	3Ch
30	Minimum Active to Precharge Time (tRAS)	40 ns	28h
31	Module Bank Density	256M of 1 row	40h
32	Address and Command Input Setup Time Before Clock	0.6 ns	60h
33	Address and Command Input Hold Time After Clock	0.6 ns	60h
34	Data/Data Mask Input Setup Time Before Data Strobe	0.4 ns	40h
35	Data/Data Mask Input Hold Time After Data Strobe	0.4 ns	40h
36-40	Reserved	Reserved	00h
41	Minimum active /auto-refresh time(tRC)	55 ns	37h
42	Minimum auto-refresh to active command period (tRFC)	70 ns	46h
43	Maximum cycle time(Tck max)	10 ns	28h
44	Maximum DQS-DQ skew time(tDQSQ)	0.4 ns	28h
45	Maximum read data hold skew factor(tQHS)	0.50 ns	50h
46-61	Reserved	Reserved	00h
62	SPD Revision	Rev0.0	00h
63	Checksum for Bytes 0-62	-	BEh
64-71	Manufacturer's JEDEC ID Code	-	7F, 7F, 7F, 58h
72	Module Manufacturing Location	-	31h
73-90	Module Part Number	BD512TEC500	42, 44, 35, 31, 32, 54, 45, 43, 35, 30, 30h
91-92	Module Revision Code	Reserved	00h
93-94	Module Manufacturing Date	YY-WW	-
95-98	Module Serial Number	Reserved	00h
99-127	Manufacturer's Specific Data	Reserved	00h
128-255	Open for customer use	Reserved	00h

PACKAGE DIMENSIONS